RK2918
Technical Reference Manual
Brief

Revision 0.2
Nov 2010

Revision History

Date	Revision	Description
2010-9-5	0.1	Initial Release
2010-10-1	0.2	Add package information

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Chapter 1 Introduction

1.1 Overview

RK2918 is a high-performance, highly-integrated, low-power digital multimedia processor which is based on Contex – A8 processor. It is designed for internet multimedia product applications such as MID, Mobile AP, Internet TV etc.

1.2 RK29 Features

- **Core and System Operation**
  - Contex A8 core with Neon, ETM/DBG
  - 32KB/32 KB L1 I/D cache
  - 512KB L2 Cache
  - System boot from Nand, eMMC, SPI Nor FlASH and UART

- **Internal Memory**
  - Embedded 16KB ROM for Boot code.
  - Embedded 16KB SRAM for low power running and general using.

- **Clock & Power Management**
  - Four on-chip PLLs for A8 subsystem, Video subsystem and Other logic
  - Power supply shut down for 11 power domain separately
    - 1. Cortex-A8 -- Core/L1 Cache
    - 2. Cortex-A8 – Neon
    - 3. Cortex-A8 -- ETM/.DBG
    - 4. Cortex-A8 -- L2 Cache
    - 5. Video encoder and decoder
    - 6. Display system
    - 7. peripheral subsystem
    - 8. Mini system (Timer+GPIO+GIC+Dynamic memory interface+Internal memory+DMAC+UART + I2C)
    - 9. GPU
    - 10. Always on logic(SCU+PMU+IOMUX)
    - 11. RTC

- **Interrupt Controller**
  - ICU (Interrupt Control unit) integrated inside DSP subsystem
    - Support software interrupt generation
    - 70 interrupt sources supported
    - support interrupt priority level configurable
    - support fiq and irq output (low level sensitive)
    - interrupt source is only high level sensitive
    - Support security extension

- **External Memory Interface**
  - DDR II and Mobile DDR Memory controller
    - Max frequency:400MHz(DDRII) and 200MHz(Mobile DDR)
    - 32bit/16bit data bus width
    - 7 data port with 64bits AXI bus
    - Support four chip selects, each is up to 512MB
    - support separately asynchronous FIFO for every port
    - support async clock among bus of every port
    - Hardmacro DDR PHY,including Combo IO
  - Static Memory controller

- Sync/Async SRAM and Nor Flash supported
- AXI 64bits slave interface
- 8bits/16bits data bus width
- Support four chip selects, each is up to 16MB
- Support shared and separated data and address bus

- Nand Flash controller
  - Support 8bits/16bits Flash and 8bits Sync DDR Flash
  - Support LBA/Clear Nand/ E2Nand Flash
  - Support ONFI interface
  - Support up to 8 chip selects
  - Support AHB Master interface and AHB Slave interface
  - 16bit/1KB ECC, compatible with 8bit/512B
  - 24bit/1KB ECC, compatible with 12bit/512B
  - Support DLL bypass and 1/4 or 1/8 clock adjust in DDR Nand
  - Support configurable timing on the interface
  - Support internal DMA operation

- SD/MMC controller
  - Support SD2.0 / MMC4.2 / SDIO1.1 /HS-MMC interface
  - Two controller integrated, one for SD/MMC, Another for SDIO
  - Support 1bit/4bit/8bit data width
  - Programmable baud rate , support card clock rate up to 52MHz
  - support 4 channel
  - DMA-based data transfer supported

- iNand and eMMC controller
  - support iNand and eMMC interface
  - support boot

- **DMA Controller**
  - Three DMA Controllers in chip
  - DMA Controller 0
    - One 64bits AXI master interface
    - Two APB slave interface:one for non-secure, another for secure
    - Only support transfer data between memory
    - An instruction set provides flexibility for DMA transfer
    - Support scatter-gather transfer function
    - Support 3 channel totally
    - support interrupt output signals
    - Used for data transfer among internal memory,external static/dynamic memory,nand flash,buffer inside hif
  - DMA Controller 1
    - One 64bits AXI master interface
    - Only one APB slave interface for non-secure
    - Support transfer data between memory and peripheral,memory and memory
    - An instruction set provides flexibility for DMA transfer
    - Support scatter-gather transfer function
    - Support 4 channel totally
    - support interrupt output signals
    - Up to 8 peripheral hardware request
    - Used for data transfer for I2S & SPDIF & PCM audio interface and Uart0
  - DMA Controller 2
    - One 32bits AXI master interface
    - one APB slave interface for non-secure
    - Support transfer data between memory and peripheral, memory and memory

- An instruction set provides flexibility for DMA transfer
- Support scatter-gather transfer function
- Support 6 channel totally
- support interrupt output signals
- Up to 20 peripheral hardware request
- Used for data transfer for Uart,SPI,SD/MMC,SDIO,HSADC,MAC

- **Video processor unit**
  - Video decoder
    - Multi-format full-HD video decoder, including H264/MPEG-4/MPEG-2 /VC1 /RV/MPEG-1/H263/DivX/Sorenson Spark/VP8/AVS Stream
    - Maximum decoder output size is up to 1920x1080
    - High definition-buffering for one reference picture
    - Please check another sheet for detailed features
  - Video encoder
    - Support H264 (baseline/Main/High profiles,Levels 1~4) format video encoder
    - Maximum image size is up to 1920x1080
    - Maximum frame rate is up to 30fps
    - Bit rate is from 10Kbps to 20Mbps
    - Please check another sheet for detailed features
- **Image processor unit**
  - GPU
    - Support OpenGL ES2.0,OpenGL ES1.1 and OpenVG graphics standards
    - Geometry Rate is 10Mtri/s
    - Depth-only Pixel Rate is 200MPix/s
    - Textured Pixel Rate is 100Mpix/s
    - Vertex Rate is 50Mvert/s
  - JPEG encoder
    - Compatible with JFIF file format 1.02 for output data
    - Output data format is interleaved only
    - Input data format is YCbCr(4:2:0;4:2:2) and RGB/BGR (444,555, 565,888, 101010)
    - Supported image size is up to 4672x3504
    - Maximum data rate is up to 90million pixels/s
    - Support RGB 8bits,24bits and JPEG compressed thumbnails
  - JPEG decoder
    - Compatible with JFIF file format 1.02 for input data
    - input sampling formats are YCbCr 4:0:0,4:2:0,4:2:2,4:4:0,4:1:1 and 4:4:4
    - Ouput data formats are YCbCr 4:0:0,4:2:0,4:2:2,4:4:0,4:1:1 and 4:4:4 semi planar
    - Supported image size is up to 8176x8176
    - Maximum data rate is up to 76million pixels/s at 200MHz
    - JPEG compressed thumbnails supported
    - Error detection supported
  - Pre-processor
    - Support the following color space conversion RGB(any composite) to YCbCr4:2:0 with BT601 or BT709 or any user defined coefficients
    - YCbCr4:2:2 to YCbCr4:2:0
    - Cropping size is from 4672x3504 to any supported encoding size
    - Support 90 or 270 degrees rotation
    - Support video stabilization and scene detection

- Post-processor
  - Multiple format input and output data supported
  - Input image source is from video decoder or software decoder or camera interface
  - Input image size is up to 8176x8176 in pipelined mode
  - Output image size is up to 1920x1080 or rotated
  - Support VC1 range mapping function and MPEG4 deblocking filter
  - Support arbitrary non-integer image scale up by up to 3x size with bicubic polynomial interpolation method
  - Support arbitrary non-integer scale down (unlimited down size) with averaging filter method

- **VIDEO interface**
  - Display controller
    - Image post processor
      - De-interlace for I2P（YCbCr422, YCbCr420-0 mode, up to 1080p）
      - Pre scaling:
        - 1/2~1/8 integer linear down-scaling
        - Support RGB565、RGB888、YCbCr422、YCbCr420
      - Post scaling:
        - 1/2~ 1 non-integer down-scaling
        - 1~ 8 up-scaling
      - Support RGB565、RGB888、YCbCr422、YCbCr420
      - Rotation: 270-degrees, 90-degrees(YCbCr & RGB)
    - Display interface
      - Parallel RGB LCD Interface: 24-bit(RGB888), 18-bit(RGB666), 15-bit(RGB565)
      - Serial RGB LCD Interface: 3x8-bit(RGB delta support), 3x8-bit + dummy,16-bit + 8-bit
      - MCU LCD interface: i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
      - TV Interface: ITU-R BT.656/720P/1080I
    - Display overlay
      - One Background layer: programmable 24-bit color
      - One Video layer(win0):
        - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420-0, YCbCr420-1
        - Maximum resolution is 1920x1080
        - Virtual display(roller support)
        - 8-bit alpha blending
        - Transparency color key
        - Rotation: X mirror, Y mirror
        - Post-scale: 1~1/2 down-scaling, 1~8 up-scaling, horizontal 4-taps, vertical 2-taps
        - Sharp/smooth filter
      - One Graphic layer(win1):
        - RGB888, ARGB888, RGB565
        - Maximum resolution is 1920x1080
        - Virtual display(roller support)
        - 8-bit alpha blending
        - Transparency color key
      - One OSD layer(win2):
        - 1/2/4/8bpp palette mode
        - Maximum resolution is 1920x1080
        - 8-bit alpha blending
        - Transparency color key

- Hardware cursor(HWC):
  - 32x32x2bpp (bit per pixel)
  - 3-color and transparent mode*(add 2-color + transparency + tran_invert)
  - 4-bit alpha blending
- Others feature
  - 3 x 256 x 8 bits LUTs (Contrast, Brightness,Gamma)
  - Graphic layer and Video layer overlay exchangeable
  - YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YCbCr modules
  - Replication(16-bit to 24-bit) and Dithering(24-bit to 16-bit/18-bit)
  - Blank and black display, all white display
  - Standby mode

- EPD display controller
  - Stardard EPD display drvier
  - Support PVI, AUO EPD

- Video input interface
  - Support 8bits CCIR656 PAL/NTSC interface
  - Support 10bits/12bits Raw data interface
  - Maximum frequency is up to 96MHz
  - Embedded DMA interface as AXI 64bits master

- **Audio interface**
  - I2S/PCM0
    - Support 16bits~32bits audio data resolution
    - Support up to 8 channel for transfer data and 2 for receive
    - Maximum Sample resolution is up to 192KHz
    - Support I2S,Left-justified and right-justified mode
    - Support I2S and PCM mode selection for every channel
    - Support Interrupt-based or DMA-based mode

  - I2S/PCM1
    - Support 16bits~32bits audio data resolution
    - Support 2 channel for transfer data and 2 for receive
    - Maximum Sample resolution is up to 192KHz
    - Support I2S,Left-justified and right-justified and PCM mode
    - Support Interrupt-based or DMA-based mode

- **USB controller**
  - Three USB controller embed in SOC
  - Two USB 2.0 Hi-speed OTG controller
  - One USB 1.1 Full-speed host controller

- **TS stream interface**
  - 2bits data bus for GPS interface
  - 10bits high-speed TS interface for Mobile TV
  - support pid filter function

- **MAC controller**
  - Support MII and RMII interface

- **Low_speed Peripheral interface**
  - Two Serial Peripheral Interface (SPI) Controller
    - Support both master and slave mode
    - Support Interrupt-based or DMA-based mode

- Four transfer protocols available with selectable clock polarity and clock phase
- Different bit rates available for SCLK
- Bi-direction mode

- Four UART
  - Support interrupt-based or DMA-based mode
  - UART0/1/2/3 support 115.2Kbps,460.8Kbps,921.6Kbps,1.5Mbps,3Mbps , up to 4Mbps
  - UART1 support infrared(IR) transmit/receive
  - UART0&UART2&UART3 support Auto flow-control
  - UART input clock can operate at a higher speed
  - Each UART contains two 32byte FIFOs for data receive and transmit
  - support programmable baud rates
  - Standard asynchronous communication bits (start, stop and parity)

- Four I2C controller
  - Support Multi masters operation
  - Software programmable clock frequency and transfer rate up to 400Kbit/sec
  - Supports 7 bits and 10 bits addressing modes

- Audio interface - I2S/PCM0
  - Support 16bits~32bits audio data resolution
  - Support up to 8 channel for transfer data and 2 for receive
  - Maximum Sample resolution is up to 192KHz
  - Support I2S,Left-justified and right-justified mode
  - Support I2S and PCM mode selection for every channel
  - Support Interrupt-based or DMA-based mode

- Audio interface -I2S/PCM1
  - Support 16bits~32bits audio data resolution
  - Support 2 channel for transfer data and 2 for receive
  - Maximum Sample resolution is up to 192KHz
  - Support I2S,Left-justified and right-justified and PCM mode
  - Support Interrupt-based or DMA-based mode

- PWM
  - Built-in three 32 bit timer modulers
  - Programmable counter
  - Chained timer for long period purpose
  - 4-channel 32-bit timer with Pulse Width Modulation (PWM)
  - Programmable duty-cycle, and frequency output

- General Purpose IO (GPIO)
  - 7 groups of GPIO, totally 176
  - In power down mode, GPIO status can be controlled by another registers in always on domain

- Timers in CPU system
  - Built-in Three 32 bits timer modules
  - input clock is programmable, fixed clock or divided from bus clock

- Watchdog Timer (WDT)
  - Watchdog function (Generate a system reset or an interrupt)
  - Built-in 32 bits programmable counter

- **Analog IP interface**
  - ADC Converter

- 3-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
- No off-chip components required
- DNL less than +/-1 LSB , INL less than +/-1.5 LSB

- eFUSE functions
  - Embed 128 bit one time programmed eFuse

- Max Frenquency
  - TBD

1.3 Package

- RK2918 TFBGA512，16mmX16mm, 0.65mm Pitch